Junseo Lee

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Research Interests

My research interests are in **GPU microarchitecture** and **the architectural support for emerging workloads**, particularly vision/graphics tasks such as neural rendering.

- **Keywords**: Computer Architecture, GPU Microarchitecture, Hardware-Software Co-Design for Emerging Applications, Computer Vision/Graphics

Education

Seoul National University — Seoul, Republic of Korea

M.S./Ph.D., Electrical and Computer Engineering — Mar 2022 – Present
- Computer Architecture and Systems Lab (Advisor: Prof. Jaewoong Sim)

B.S., Electrical and Computer Engineering — Mar 2018 – Feb 2022

Research Experience

Graduate Research Assistant — Mar 2022 - Present
Seoul National University — Seoul, Republic of Korea

- Advisor: Prof. Jaewoong Sim
- Worked on algorithm-hardware co-design to efficiently execute Neural Radiance Fields (NeRF) rendering.
  - Proposed **NeuRex**, an algorithm-hardware co-design that achieves significant speedups compared to GPUs.
  - Co-designed a restricted hashing algorithm and an encoding engine that eliminate irregular off-chip memory accesses in the encoding stage.
  - Implemented NeuRex in SystemVerilog, demonstrating small area overhead and low power consumption.
- Worked on designing hardware architecture to efficiently support 3D Gaussian splatting (3DGS) rendering.
  - Designed **GSCore**, a specialized accelerator that efficiently executes 3D Gaussian splatting rendering pipeline.
  - Proposed three algorithmic optimizations and tailored hardware to reduce ineffective computations.
  - Showed that the proposed algorithmic optimizations improve GPU rendering performance by $2\times$.
- Worked on extending hardware graphics pipeline in modern GPUs to accelerate volume rendering.
  - Proposed **VR-Pipe**, a hardware extension for modern GPU graphics pipelines to reduce the pressure on the fixed-function blending unit (ROP).
  - Designed two innovations to effectively reduce the number of fragments processed by programmable/fixed-function units in the early stages of the rendering pipeline.

Publications

VR-Pipe: Streamlining Hardware Graphics Pipeline for Volume Rendering
Junseo Lee, Jaisung Kim, Junyong Park, Jaewoong Sim
*Proc. of the 31st International Symposium on High Performance Computer Architecture (**HPCA**), March 2025*

GSCore: Efficient Radiance Field Rendering via Architectural Support for 3D Gaussian Splatting
Junseo Lee, Seokwon Lee, Jungi Lee, Junyong Park, Jaewoong Sim
*Proc. of the 2024 International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), April 2024*

NeuRex: A Case for Neural Rendering Acceleration
Junseo Lee, Kwanseok Choi, Jungi Lee, Seokwon Lee, Joonho Whangbo, Jaewoong Sim
*Proc. of the 50th International Symposium on Computer Architecture (**ISCA**), June 2023*

Teaching

Graduate Research Assistant
Seoul National University — Seoul, Republic of Korea

- ECE 315.A: Digital Systems Design and Experiments
- ECE 322: Computer Organization

Led lab sessions and the final project that implements a CNN accelerator in RTL on FPGA (ECE 315.A).
Prepared the assignments, such as a C++-based cycle-level cache simulator (ECE 322).

Skills

Languages: C/C++, CUDA, Python, Verilog/System Verilog, GLSL

Tools: PyTorch, Intel VTune, Nsight Compute/Graphics/Systems

APIs: OpenGL, Vulkan, OptiX